

SV6256P

Single-Chip Dual Band 802.11 a/b/g/n MAC/BB/Radio with SDIO Interface

General Description

The SV6256P is a low-power single chip device providing for the highest level of integration for internet of thing embedded systems. It is designed to support all mandatory IEEE 802.11b data rates of 1, 2, 5.5 and 11 Mbps, all 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps, as well as 802.11n MCS0~MCS7, HT20/HT40, 800ns and 400ns guard interval.

It includes a dual band WLAN CMOS efficient power amplifier (PA) and an internal low noise amplifier (LNA). The Radio Frequency Front-end is single-ended bi-directional input and output.

The SV6256P has additional LDOs and DCDC buck convertor that could provide noise isolation for digital and analog supplies and excellent power efficient with minimum BOM cost.

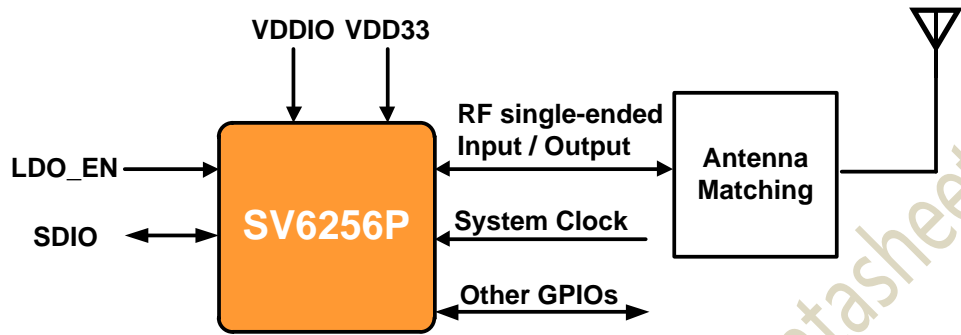
The only external clock source needed for SV6256P based designs is a high speed crystal or oscillator. A variety of reference clocks are supported which include 25, 40 MHz

SV6256P Features

- All CMOS IEEE 802.11 a/b/g/n single chip
- Single stream 802.11n provides highest throughput and superior RF performance for embedded system
- Advanced 1x1 802.11n features:
 - Full / Half Guard Interval
 - Frame Aggregation
 - Reduced Inter-frame Space (RIFS)
 - Space Time Block Coding (STBC)
 - Greenfield mode
- Integrated WLAN CMOS efficient power amplifier with internal power detector and closed loop power calibration

ORDERING INFORMATION

Part Number	Package
SV6256P	Green/RoHS Compliant QFN 48L, 6x6 mm, 0.4mm pitch



SV6256P System Block Diagram

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Revision History

Version	Date	Owner	Description
0.1	2018/08/7	Hoz Lin	Copy and modify from SV6156P

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1 SYSTEM OVERVIEW

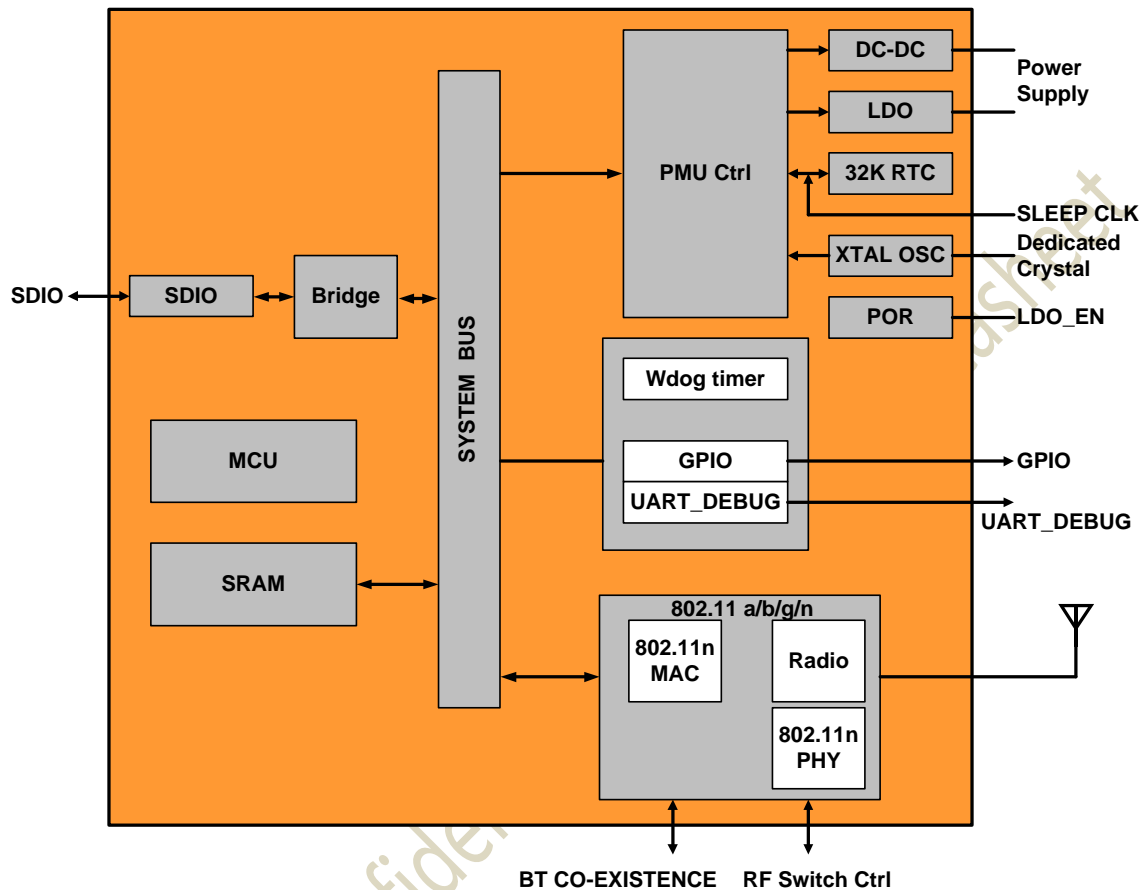


Figure 1-1: SV6256P Block Diagram

1.1 General Description

The SV6256P WLAN is designed to support IEEE 802.11 a/b/g/n single stream with the state-of-the-art design techniques and process technology to achieve low power consumption and high throughput performance to address the requirement of mobile and handheld devices. The SV6256P WLAN low power function uses the innovative design techniques and the optimized architecture which best utilizes the advanced process technology to reduce active and idle power, and achieve extreme low power consumption at sleep state to extend the battery life. The SV6256P WLAN A-MPDU Tx function maximizes the throughput performance while achieving the best buffer utilization.

1.2 MAC Features

- 802.11 a/b/g/n/e/i/d
- WLAN/BT coexistence mechanisms
- 802.11n features

- A-MPDU Tx & Rx
- Support immediate Block-Ack
- AP/STA mode
 - Soft-AP
- Rate adaption mechanism
- WFA features
 - WEP/TKIP/WPA/WPA2
 - WMM/WMM PS

1.3 PHY features

- 802.11b, 11g, and 802.11n 1T1R
- Short Guard Interval
- Greenfield mode
- RIFS in RX mode
- STBC in RX mode
- Enhanced and robust sensitivity for wider coverage range
- Supports calibration algorithm to handle no-idealities effects from CMOS RF block

1.4 HOST INTERFACE

- SDIO 2.0
 - Standard SDIO 2.0 device interface
- UART
 - Support RX/TX, 2 pins
 - Baud rate up to 921600

1.5 System Clocking and Reset

The SV6256P has a system clocking block and reset which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consist of clock enable and power signals which are used to gate the clocks going to internal modules. The system clocking and reset block also manages resets going to other modules within the device.

1.6 Design for Test

It also has features which enable testing of digital blocks via ATPG scan, memories via MBIST, analog components, and the radio.

2 POWER SUPPLIES AND POWER MANAGEMENT

2.1 General Description and PMU Power Connection

The power management unit (PMU) contains Under-Voltage Lockout (UVLO) circuit, Low Dropout Regulators (LDOs), buck DC-DC converter and reference bandgap circuit.

The PMU integrated multi-LDOs and one buck converter. Those circuits are optimized for the given functions by balancing quiescent current, dropout voltage, line / load regulation, ripple rejection and output noise.

The input voltage of the buck converter is 3.3V. Its output voltage is 1.6V and feeds into the input power of the RF circuit and DLDO which has 1.2V output voltage for all digital circuits.

Figure 2-1 shows the typical power connection for SV6256P. DLDO and some RF circuits are powered by the buck converter output. The VDDIO is a power input which may be 1.8V or 3.3V from the host side. The connection structure is shown in the figure below.

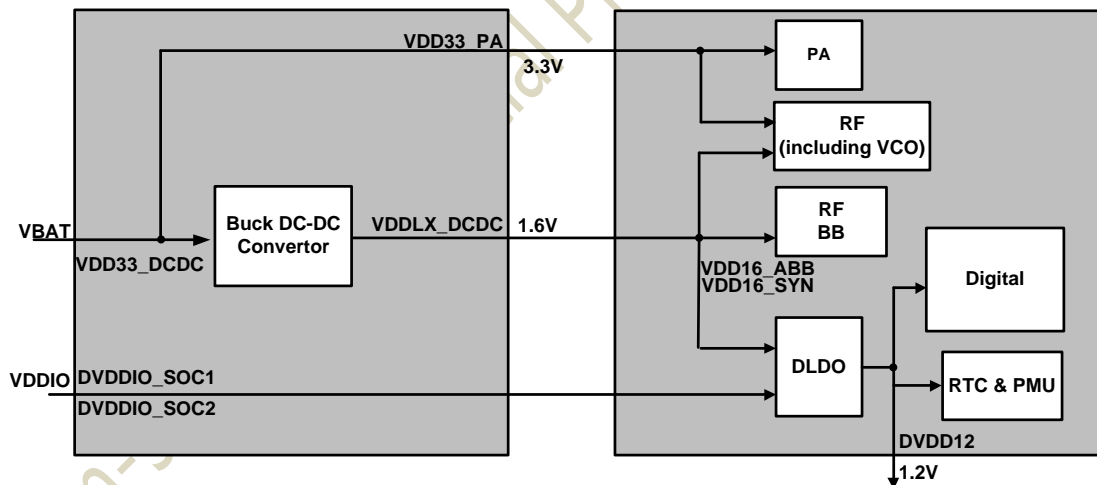


Figure 2-1: SV6256P Power Connection

2.2 Under-Voltage Lockout (UVLO)

The UVLO state in the PMU prevents startup if the initial voltage of the battery is below pre-defined threshold. It ensures that SV6256P is powered on with the battery in good condition. In addition, when the battery voltage is getting lower, it will enter the UVLO state, and the PMU will be turned off by itself to prevent further discharging.

2.3 DLDO

The DLDO is integrated in the PMU to supply digital core. It converts voltage from 1.6V input to 1.2V output which suits the digital circuits. The input is typically connected to the buck's output.

2.4 Buck Converter

The regulator is a DC-DC step-down converter (buck converter) to source 300mA (max.) with 2.0V to 1.5V programmable output voltage based on the register setting. It supplies power for the RF circuit and DLDO.

2.5 Power Management Control

There are three power modes that SV6256P operates when it is initialized: HOST_OFF, ACTIVE mode and SLEEP mode. There are two intermediate system transition modes: FW_DOWNLOAD and WARM_UP mode. The following are the brief introduction to each mode.

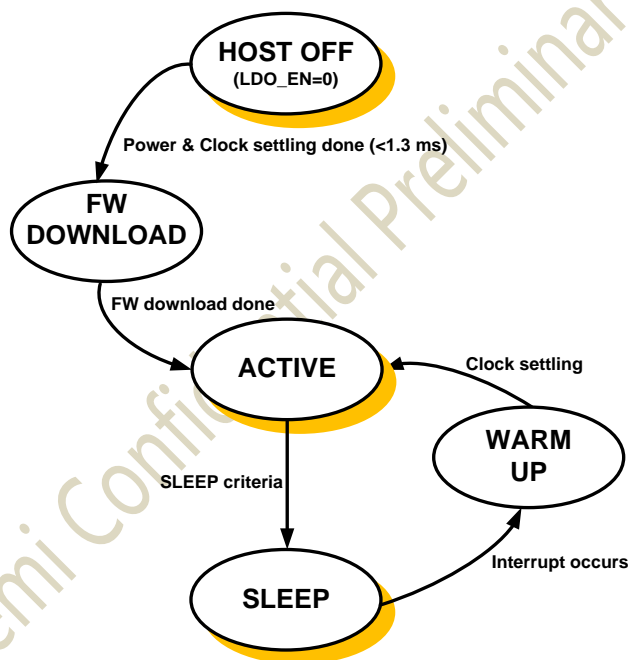


Figure 2-2: SV6256P Power State

Table 2-1: SV6256P Power State Description

State	Description
HOST OFF	When LDO_EN pin is de-asserted and logically low, the chip is brought to this state immediately.
	Sleep clock and internal power supply is disabled.
	After LDO_EN pin is asserted, the internal power and clock will be settled down within 1.3 ms.
FW DOWNLOAD	States for firmware download after power and clock is settled down.
SLEEP	The host controller can determine when to enter sleep to turn off most circuit in SV6256P. All the RF, DPLL circuits are turned off. In sleep mode, the system could be awakened after the sleep time is expired or by an external wake up signal from the host controller.
	All internal states are maintained and the Crystal oscillator is disabled.
WARM UP	The system transitions from SLEEP to ACTIVE. The crystal or oscillator is brought up and the PLL is enabled.
ACTIVE	The high speed clock is operational and sent to each block by the clock control register.
	The RF circuit is enabled to transmit or receive data, and the whole system is under normal operation.

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2.6 Power-on Sequence

Figure 2-3 shows the power-on sequence of the SV6256P from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. The LDO_EN input level must be kept the same as VDDIO voltage level. After initial power-on, the LDO_EN signal can be held low to turn off the SV6256P or pulsed low to induce a subsequent reset. After LDO_EN is assert and host starts the power-on sequence of the SV6256P. From that point, the typical SV6256P power-on sequence is shown below:

1. Within 1.3 millisecond, the internal power-on reset (POR) will be done. And host could download firmware code. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.

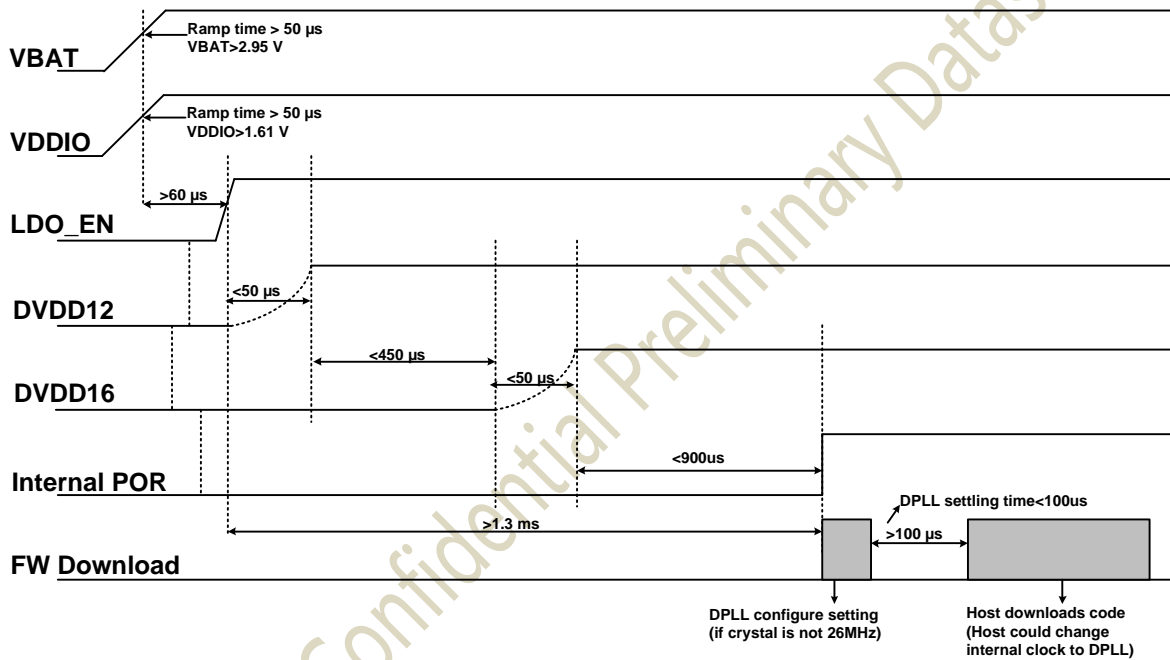


Figure 2-3: Power-on sequence

2.7 Reset Control

The SV6256P LDO_EN pin can be used to completely reset the entire chip. After this signal has been de-asserted, the SV6256P is in off mode waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules are held in reset. Once the host has initiated communication, the SV6256P turns on its crystal and later on DPLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

3 INTERFACE DESCRIPTION

3.1 SDIO Timing Waveform

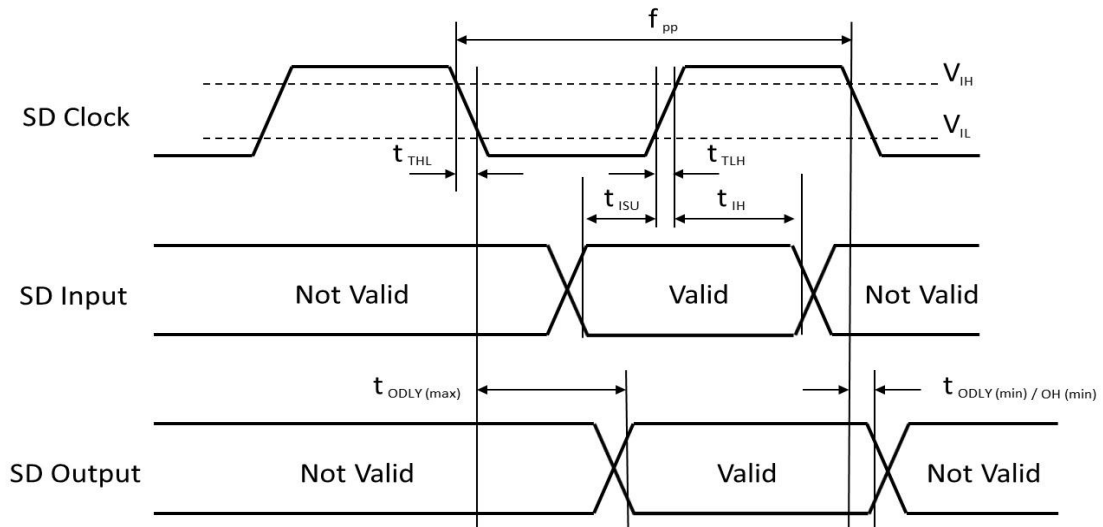


Table 3-1: SV6167Q SDIO version 2.0 Timing Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Clock CLK (All values are referred to min(V_{IH}) and max (V_{IL})).					
f_{pp}	Clock frequency Data Transfer Mode	0		50	MHz
t_{TLH}	Clock rise time			3	ns
t_{THL}	Clock fall time			3	ns
Inputs CMD, DAT (reference to CLK)					
t_{ISU}	Input set-up time	6			ns
t_{IH}	Input hold time	2			ns
Outputs CMD, DAT (reference to CLK)					
t_{ODLY}	Output Delay time during Data Transfer Mode			14	ns
t_{OH}	Output Hold time	2.5			Ns

4 DC CHARACTERISTICS

4.1 Absolute Maximum Ratings

The absolute maximum ratings in Table 3-1 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 3-1: Absolute Maximum Ratings

Table 3-1: Absolute Maximum Ratings

Symbol (domain)	Description	Max Rating	Unit
VDD16	VDD input for analog 1.6V	-0.3 to 3.6	V
VDD33_SX	VDD input for external components I/O control	-0.3 to 3.6	V
VDD33_SX_5G	VDD input for external components I/O control	-0.3 to 3.6	V
VDD33_RF	VDD input for external components I/O control	-0.3 to 3.6	V
DVDDIO1	VDD input for GPIO pins	-0.3 to 3.6	V
DVDDIO2	VDD input for GPIO pins (same level as DVDDIO1)	-0.3 to 3.6	V
DVDDIO3	VDD input for GPIO pins (same level as DVDDIO1)	-0.3 to 3.6	V
DVDD12	VDD output for internal digital circuit	-0.3 to 1.32	V
VDD16_DCDC	VDD input for digital circuit's LDO	-0.3 to 3.6	V
VDD33_DCDC	VDD input for DCDC	-0.3 to 3.6	V
VDD33_SX	VDD input for external components I/O control	-0.3 to 3.6	V
VDD33_SX_5G	VDD input for external components I/O control	-0.3 to 3.6	V

4.2 Environmental Ratings

The environmental ratings are shown in Table 3-2

Table 3-2 Environmental Ratings

Characteristic	Conditions/Comments	Value	Units
Ambient Temperature (T_A)	Functional operation	-20 to +85	°C

4.2.1 Storage Condition

The calculated shelf life in sealed bag is 12 months if stored between 0°C and 40°C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- a) Mounted within 168-hours of factory conditions < 30 °C /60%RH
- b) Storage humidity needs to maintained at <10% RH
- c) Baking is necessary if customer exposes the component to air over 168 hrs, baking condition: 125°C / 8hrs

4.3 Thermal Characteristics

Table 3-3: the thermal characteristics of the SV6256P

Thermal characteristics without external heat sink in still air condition

Symbol	Description	Typ.	Unit
T _J	Maximum Junction Temperature (Plastic Package)	125	°C
θ _{JA}	Thermal Resistance θ _{JA} (°C/W) for JEDEC 4L system PCB	37.8	°C/W
θ _{JC}	Thermal Resistance θ _{JC} (°C/W) for JEDEC 4L system PCB	TBD	°C/W
Ψ _{Jt}	Thermal Characterization parameter Ψ _{Jt} (°C/W) for JEDEC 4L system PCB	4.13	°C/W
	Maximum Lead Temperature (Soldering 10s)	260	°C

Notes: * JEDEC 51-7 system FR4 PCB size: 3" x 4.5" (76.2 x 114.3 mm)

* Thermal characteristics without external heat sink in still air condition

4.4 PMU Under Voltage Lock-out (UVLO) Characteristics

Table 3-4 PMU UVLO characteristics

Symbol (domain)	Description	Min.	Typ.	Max.	Unit
Under Voltage Lock-Out (UVLO)					
Under voltage rising threshold of VBAT	VDD33: pin VDD33_DCDC & VDD33_RF		2.95		V
Under voltage falling threshold of VBAT	VDD33: pin VDD33_DCDC & VDD33_RF		2.85		V
Under voltage rising threshold of DVDDIO	DVDDIO: pin DVDDIO_SOC1 & DVDDIO_SOC2		1.6		V
Under voltage falling threshold of DVDDIO	DVDDIO: pin DVDDIO_SOC1 & DVDDIO_SOC2		1.5		V

4.5 Electrostatic Discharge Specifications

This is an ESD sensitive product! Observe precaution and handle with care. Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices.

Table 3-5: ESD Specifications

Pin Type	Test Condition	ESD Rating	Unit
Human Body Mode (HBM)	refers to MIL-STD-883G Method 3015.7	Pass ± 2.5	KV
CDM		Pass ± 500	V

4.6 Recommended Operating Conditions and DC Characteristics

Table 3-6: Recommended Operating Conditions and DC Characteristics

Domain (Symbol)	Description	Min.	Typ.	Max.	Unit
VDD16	VDD input for analog 1.6V		1.6		V
VDD33_SX	VDD input for external components I/O control	3.13	3.3	3.46	V
VDD33_SX_5G	VDD input for external components I/O control	3.13	3.3	3.46	V
VDD33_RF	VDD input for external components I/O control	3.13	3.3	3.46	V
DVDDIO1	VDD input for GPIO pins	3.13	3.3	3.46	V
DVDDIO2	VDD input for GPIO pins (same level as DVDDIO1)	3.13	3.3	3.46	V
DVDDIO3	VDD input for GPIO pins (same level as DVDDIO1)	3.13	3.3	3.46	V
DVDD12	VDD output for internal digital circuit		1.2		V
VDD16_DCDC	VDD input for digital circuit's LDO		1.6		V
VDD33_DCDC	VDD input for DCDC	3.13	3.3	3.46	V
(V _{IL})	Input Low voltage when VDDIO=3.3V	-0.3		0.8	V
(V _{IH})	Input High voltage when VDDIO=3.3V	2		3.6	V
(V _{T+})	Schmitt trigger low to high threshold voltage when VDDIO=3.3V	1.6	1.74	1.89	V
(V _{T-})	Schmitt trigger high to low threshold voltage when VDDIO=3.3V	1.27	1.4	1.56	V

(V_{OL})	Output low voltage when VDDIO=3.3V			0.4	V
(V_{OH})	Output high voltage when VDDIO=3.3V	2.4			V
(R_{PD})	Input weakly pull-down resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull- down option except that GPIO_5 has internal weakly pull-up option				KΩ
(R_{PU})	Input weakly pull-high resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull- down option except that GPIO_5 has internal weakly pull-up option				KΩ
(I_{OL})	Low level output current @ V _{OL} (max), 8mA setting	11.9	17.7	23.4	mA
	Low level output current @ V _{OL} (max), 12mA setting	15.8	23.5	31.1	mA
(I_{OH})	High level output current @ V _{OH} (min), 8mA setting	17.2	34.1	58.8	mA
	High level output current @ V _{OH} (min), 12mA setting	23.9	47.2	81.5	mA

5 FREQUENCY REFERENCES

5.1 Crystal Oscillator Specifications

Table 5-1: Crystal Oscillator Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range	–	25,40 MHz			
Crystal load Capacitance	–	–	10		pF
ESR	–	–	–	70	Ω
Frequency tolerance Initial and over temperature	–	-20ppm	–	20ppm	ppm

5.2 External Clock-Requirements and Performance

Table 5-2: External Clock-Requirements and Performance

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range	–	25,40 MHz			
OSCIN Input Voltage	AC-couple analog signal	400	–	1500	mV _{PP}
Frequency tolerance Initial and over temperature	–	-20ppm	–	20ppm	ppm
Duty Cycle	25MHz clock	40	50	60	%
Phase Noise (802.11b/g)	25MHz clock at 1KHz offset	–	–	-119	dBc/Hz
	25MHz clock at 10KHz offset	–	–	-129	dBc/Hz
	25MHz clock at 100KHz offset	–	–	-134	dBc/Hz
	25MHz clock at 1MHz offset	–	–	-139	dBc/Hz
Phase Noise (802.11n 2.4GHz)	25MHz clock at 1KHz offset	–	–	-125	dBc/Hz
	25MHz clock at 10KHz offset	–	–	-135	dBc/Hz
	25MHz clock at 100KHz offset	–	–	-140	dBc/Hz
	25MHz clock at 1MHz offset	–	–	-145	dBc/Hz

6 Electrical Specifications

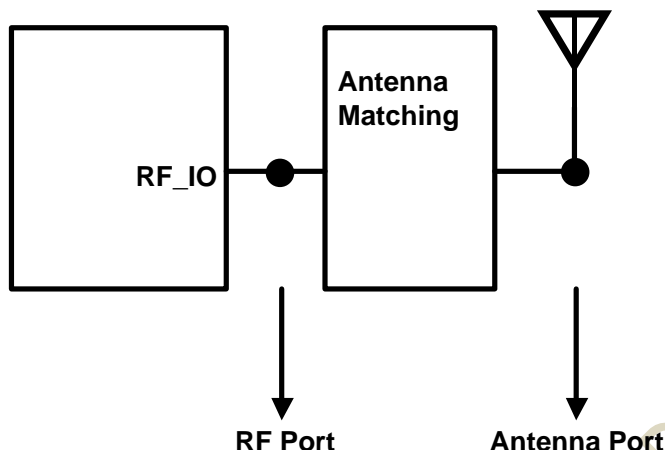


Figure 6-1: RF Front-End Reference Topology for RF Performance

Note: All specifications are measured at the Antenna Port unless otherwise specified.

6.1 WLAN RF Performance Specifications

Table 6-1: WLAN RF Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range		2412	-	2484	MHz
Rx Sensitivity (CCK)	CCK, 1 Mbps		-95.5		dBm
	CCK, 2 Mbps		-93.5		dBm
	CCK, 5.5 Mbps		-91.0		dBm
	CCK, 11 Mbps		-88.0		dBm
Rx Sensitivity (OFDM)	OFDM, 6 Mbps		-91.5		dBm
	OFDM, 9 Mbps		-90.0		dBm
	OFDM, 12 Mbps		-88.0		dBm
	OFDM, 18 Mbps		-86.0		dBm
	OFDM, 24 Mbps		-82.5		dBm
	OFDM, 36 Mbps		-79.5		dBm
	OFDM, 48 Mbps		-74.5		dBm
Rx Sensitivity (HT20) Greenfield 800nS GI Non-STBC	HT20, MCS0		-91.0		dBm
	HT20, MCS1		-88.0		dBm
	HT20, MCS2		-86.0		dBm
	HT20, MCS3		-81.5		dBm
	HT20, MCS4		-79.0		dBm
	HT20, MCS5		-74.5		dBm
	HT20, MCS6		-73.5		dBm
	HT20, MCS7		-72.5		dBm

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
RX Adjacent Channel Rejection (CCK)	CCK, 1 Mbps (30 MHz offset)		41		dB
	CCK, 11 Mbps (25 MHz offset)		41		dB
RX Adjacent Channel Rejection (OFDM)	OFDM, 6 Mbps (25 MHz offset)		39		dB
	OFDM, 54 Mbps (25 MHz offset)		23		dB
RX Adjacent Channel Rejection (HT20)	HT20, MCS0 (25 MHz offset)		38		dB
	HT20, MCS7 (25 MHz offset)		21		dB
TX Output Power	CCK, 1-11 Mbps		19		dBm
	OFDM, 54 Mbps		16		dBm
	HT20, MCS7		15		dBm

7 System Power Consumption

Note: All results are measured at the condition that VIO and VBAT are 3.3V.

Table 7-1: Power Consumption at DCDC mode (DCDC buck convertor is enable)

WLAN Operational Modes	Typ.	Unit
OFF ^a	2	uA
Rx, CCK, 1 Mbps	60	mA
Rx, OFDM, 54 Mbps	67	mA
Rx, HT20, MCS7	67	mA
Rx, HT40, MCS7	75	mA
Rx, 5.18G HT20, MCS7	88	mA
Rx, 5.805G HT20, MCS7	88	mA
Rx, 5.18 G HT40, MCS7	97	mA
Rx, 5.805G HT40, MCS7	97	mA
Tx, CCK, 1 Mbps	282	mA
Tx, 11B, 11 Mbps@18dBm	315	mA
Tx, OFDM, 54 Mbps	265	mA
Tx, HT20, MCS7	268	mA
Tx, HT40, MCS7	272	mA
Tx, 5.18 G HT20, MCS7	330	mA
Tx, 5.805G HT20, MCS7	293	mA
Power-saving(MCU_on) ^b , DTIM1	TBD	mA
Power-saving(MCU_on) ^b , DTIM3	TBD	mA
Power-saving(MCU_off) ^c , DTIM1	TBD	mA
Power-saving(MCU_off) ^c , DTIM3	TBD	mA

Table 7-2: Power Consumption at LDO mode (DCDC buck convertor is disable)

WLAN Operational Modes	Typ.	Unit
OFF ^a	2	uA
Rx, CCK, 1 Mbps	91	mA
Rx, CCK, 11 Mbps	98	mA
Rx, OFDM, 54 Mbps	111	mA
Rx, 2.4G HT20, MCS7	111	mA
Rx, 2.4G HT40, MCS7	129	mA
Rx, 5.18G HT20, MCS7	139	mA
Rx, 5.805G HT20, MCS7	139	mA
Rx, 5.18 G HT40, MCS7	156	mA
Rx, 5.805G HT40, MCS7	156	mA
Tx, CCK, 1 Mbps@18dBm	329	mA
Tx, OFDM, 54 Mbps@15dBm	296	mA
Tx, HT20, MCS7@15dBm	298	mA
Tx, HT40, MCS7@14dBm	307	mA
Power-saving(MCU_on) ^b , DTIM1	TBD	mA
Power-saving(MCU_on) ^b , DTIM3	TBD	mA
Power-saving(MCU_off) ^c , DTIM1	TBD	mA
Power-saving(MCU_off) ^c , DTIM3	TBD	mA

a. OFF mode test condition: VBAT=3.3V, VIO=3.3V, LDO_EN=0V.

b. Intra-beacon Sleep when MCU is turn on.

It is used in the applications that require the CPU to be working.

c. Intra-beacon Sleep when MCU is turn off.

8 Pin Descriptions

This section contains a listing of the signal descriptions (see Figure 7-1 for the SV6256P QFN package pin-out)

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name, indicates the negative side of a differential signal

The following nomenclature is used for signal types described in Table 6-1:

IA	Analog input signal
I	Digital input signal
IO	Digital bidirectional signal
IOA	Analog bidirectional signal
O	Digital output signal
P	Power signal
G	Ground signal

Table 8-1: SV6256P Package Pin-out

No.	Name	Description	Type (default)
1	BT_ACTIVE	BT_ACTIVE	
2	HOST_WAKE_WIFI	Host Wake Up WiFi Pin	
3	WIFI_WAKE_HOST	WiFi Wake Up Host Pin	
4	WIFI_TX_SW	WIFI_TX_SW	
5	WIFI_RX_SW	WIFI_RX_SW	
6	BT_SW	BT_SW	
7	BT_PRIORITY	BT_PRIORITY	
8	WLAN_ACTIVE	WLAN_ACTIVE	
9	GPIO05	General Purpose I/O Pins	
10	GPIO06	General Purpose I/O Pins	
11	GPIO07	General Purpose I/O Pins	
12	DVDDIO1	VIO input 1	
13	LDO_EN	Reset signal to power down IC	
14	GPIO07	General Purpose I/O Pins	
15	GPIO08	General Purpose I/O Pins	
16	GPIO09	General Purpose I/O Pins	
17	GPIO10	General Purpose I/O Pins	
18	GPIO11	General Purpose I/O Pins	
19	GPIO12	General Purpose I/O Pins	
20	DVDDIO2	VIO input 2	
21	NC	NC	
22	NC	NC	
23	VDD33_DCDC	analog 3.3V input for DCDC	
24	VDDLX_DCDC	DCDC buck regulator: output to inductor	
25	VDD16_DCDC	DCDC 1.6V	
26	DVDD12	Digital 1.2V input	
27	DVDDIO3	VIO input 3	
28	GPIO14	General Purpose I/O Pins	
29	GPIO15	General Purpose I/O Pins	
30	GPIO16	General Purpose I/O Pins	
31	GPIO17	General Purpose I/O Pins	
32	GPIO18	General Purpose I/O Pins	
33	GPIO19	General Purpose I/O Pins	
34	XTALI	Input of crystal clock reference	
35	XTALO	Output of crystal clock reference	
36	VDD33_SX	analog 3.3V input	
37	VDD16	Analog 1.6V input	
38	VDD33_SX	analog 3.3V input	
39	GND	Ground	
40	VDD33_RF	Analog 3.3V input	
41	GND	Ground	
42	NC	NC	

43	GND	Ground	
44	GND	Ground	
45	GND	Ground	
46	RF_IO	2.4 GHz RF input & output port	
47	NC	NC	
48	GND	Ground	

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9 PACKAGE INFORMATION

6 x 6 mm (body size), 0.4mm pitch QFN-48

Marking format (top view)

